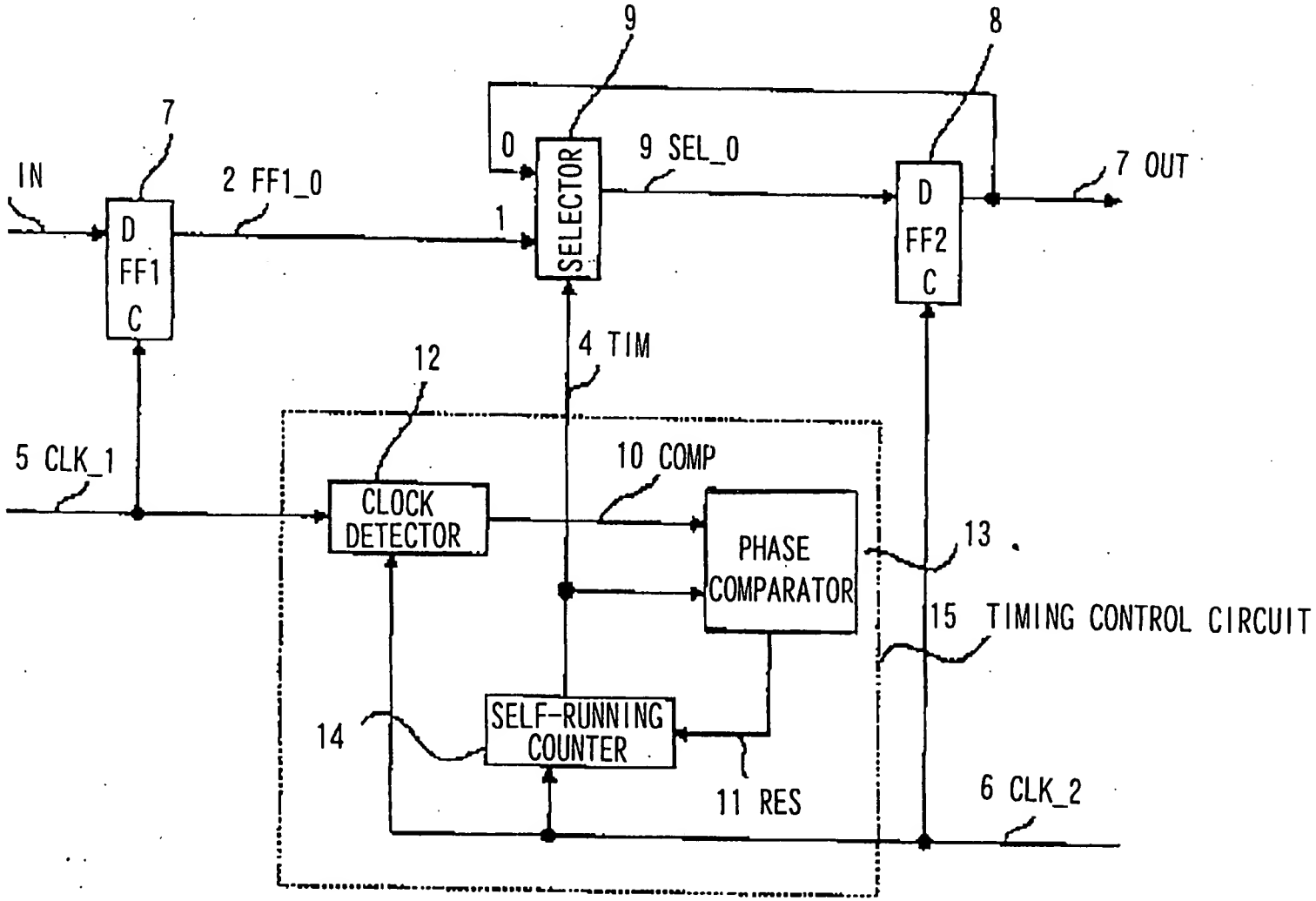
FIG . 1


9
8
7
0
9 SEL_0
7 OUT
1 IN
2 FF1_0
1
SELECTOR
D
FF1
C
D
FF2
C
4 TIM
12
5 CLK_1
10 COMP
CLOCK
DETECTOR
PHASE
COMPARATOR
13
15 TIMING CONTROL CIRCUIT
14
SELF-RUNNING
COUNTER
11 RES
6 CLK_2